REMARKS

Applicant concurrently files herewith a Petition and fee for a One-Month Extension of Time, and an Excess Claim Fee Payment Letter and fee for an excess independent claim.

Claims 1-3, 21-23, and 26-36 are all the claims presently pending in the application. Claims 5-9 and 25 have been canceled. New claims 34-36 have been added to more completely define the present invention.

Applicant gratefully acknowledges the Examiner's indication that claim 26 would be allowable if rewritten in independent form. The claim has been rewritten to overcome this rejection and to place it into condition for immediate allowance.

It is noted that the claims have been amended solely to more particularly point out Applicant's invention for the Examiner, and not for distinguishing over the prior art, narrowing the claim in view of the prior art, or for statutory requirements directed to patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 1-3, 21-23 and 27-33 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Sasaki, et al. (JP Patent No. 09-145965).(hereinafter "Sasaki").

These rejections are respectfully traversed in view of the discussion below.

I. THE CLAIMED INVENTION

Applicant's invention, as defined for example in independent claim 1, is directed to a semiconductor laser diode chip and a method for mounting the chip onto a substrate.

A feature of the present invention includes first and second measurement marks at positions relative to an active layer which are used to correctly position the chip with relation to the active layer and the measurement marks.

A further feature of the invention is that a first mark and a second mark are both on the laser diode chip.

Additionally a feature of the inventon is that the second mark is positioned oppositely to a substrate-side mark formed on the substrate.

With such features, it is possible to accurately position an LD chip to a substrate using

a passive alignment technique even when there have been errors in a production process (e.g. see page 4, lines 9-12 and page 5, lines 1-13).

An exemplary configuration of the inventive structure is shown in Fig. 5 of the application.

The conventional structures, such as those discussed below and in the Related Art section of the present application, do not have such a structure, and fail to provide for such advantages.

Indeed, such features are clearly not taught or suggested by the cited references.

II. THE PRIOR ART REFERENCES

The Examiner asserts that:

> *[regarding claims 1-6, 9, 21-25, 27-33] Sasaki et al. discloses the claimed invention. Figure 1 illustrates a semiconductor laser chip comprising a first mark, a second mark...Also note figure 2 which illustrates a first pair of marks (5) and a second pair of marks (14).*

The Examiner asserts above that Sasaki discloses the claimed invention. However, Applicant respectfully disagrees.

Specifically, in the present invention, (e.g., as defined by the non-limiting embodiments of claims 1-3, 21-23, and 27-33), both a first mark and a second mark are on the laser diode chip.

In sharp and fundamental contrast, as shown in Figs. 1-2, Sasaki discloses a first mark on the laser diode chip and the second mark on the substrate to which the chip is mounted (e.g., in Figure 1, mark 5 is on the laser diode chip and mark 14 is on the substrate.).

Furthermore, in the present invention, the second mark is positioned oppositely to a substrate-side mark formed on the substrate to overlap with each other at the mounting process (e.g., see page 14, lines 22-25 and page 15, lines 1-5 of the specification and Figs. 5-7).

However, in Sasaki the mark 5 on the laser diode chip is not positioned opposite the substrate-side mark. That is, on the substrate of Sasaki, there is no mark which is opposed to the mark on the laser diode chip. Instead, in Sasaki, the mark 5 on the laser diode chip is

positioned not to overlap to the substrate-side mark 14 (e.g., see column 4, lines 10-12; column 4, lines 35-37; column 13, lines 48-50; and Figure 4 of Sasaki). Thus, nowhere does Sasaki teach or suggest "*a second mark that satisfies a predetermined relative position relation to said first mark and is positioned oppositely to a substrate-side mark formed on said substrate*", as defined by independent claim 1 (and substantially similarly by independent claims 21 and 31).

In addition, in Sasaki even if the electrode 4a, which is upon the active layer, would have been considered a mark at the time of the invention, the mark 5 is not positioned opposite to the substrate-side mark 14.

Thus, Sasaki does not teach or suggest a first mark and a second mark which are both on the laser diode chip, and a second mark which is positioned oppositely to a substrate-side mark formed on the substrate.

Hence, turning to the clear language of independent claim 1 (and substantially similarly in independent claims 21 and 31), there is no teaching or suggestion of "*[a] semiconductor laser diode chip comprising:*

a first mark formed at a predetermined position with respect to an active layer on a face opposed to a substrate to which the chip is mounted; and

a second mark that satisfies a predetermined relative position relation to said first mark and is positioned oppositely to a substrate-side mark formed on said substrate at mounting time to said substrate,

wherein said first mark comprises a thin line formed on an upper portion of said active layer " (emphasis Applicant's).

Thus, independent claim 1 (and substantially similarly independent claims 21 and 31) is fully patentable over Sasaki.

Further, dependent claims 2-3 (and new dependent claims 34-36) when combined with independent claim 1, and dependent claims 22-23 and 27-30 when combined with independent claim 21, and 32-33 when combined with independent claim 31, respectively define additional novel and non-obvious features.

For the reasons stated above, the claimed invention is fully patentable over the cited reference.

III. FORMAL MATTERS AND CONCLUSION

The drawings have been objected to because they allegedly fail to show the positioning-type mark comprising a thin line and a measurement type mark located between the active layer and the positioning type (e.g., see page 2 of the Office Action). Applicant respectfully submits that, in view of the claim amendments above, the Examiner's objection has been overcome.

In view of the foregoing, Applicant submits that claims 1-3, 21-23, and 26-36, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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Date: 9/23/05

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